

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-6. (Canceled)

7. (Currently Amended) A circuit comprising:

a programmable logic integrated circuit comprising an embedded processor portion and a programmable logic portion, wherein the embedded processor portion includes a watchdog timer circuit; and
an external configuration source integrated circuit; that is coupled to the programmable logic integrated circuit; ~~and that stores~~ ~~storing~~ configuration information for the programmable logic integrated circuit, wherein when the watchdog timer circuit asserts a triggered signal output due to not reloading the watchdog timer circuit within a timeout period, configuration data is loaded from the external configuration source into the programmable logic integrated circuit.

8. (Original) The circuit of claim 7 wherein the external configuration source is a nonvolatile memory.

9. (Original) The circuit of claim 7 wherein the watchdog timer circuit is reloaded by periodically loading a reload register of the watchdog timer with one or more magic values.

10. (Original) The circuit of claim 7 wherein a configuration of the programmable logic portion of the programmable logic integrated circuit is held using volatile memory cells.

11. (Original) The circuit of claim 10 wherein the volatile memory cells are SRAM cells.

12. (Original) The circuit of claim 10 wherein configuration data from the external configuration source is used to configure the embedded processor portion and programmable logic portion of the programmable logic integrated circuit.

13. (Original) The circuit of claim 7 wherein the configuration is transferred serially from the external configuration source to the programmable logic integrated circuit.

14. (Original) The circuit of claim 7 wherein the watchdog timer circuit is not reloaded due to a software failure occurring within the embedded processor portion of the programmable logic integrated circuit.

15. (Original) The circuit of claim 7 wherein the watchdog circuit is not reloaded due to a power supply problem.

16. (Currently Amended) A programmable logic integrated circuit comprising:
a programmable logic portion of the integrated circuit comprising a plurality of logic array blocks, configurable to perform user logic, wherein the logic array blocks are arranged in rows and columns; and
an embedded processor portion of the integrated circuit, coupled to the programmable logic portion, comprising a watchdog timer circuit which is triggered if a count register of the watchdog timer circuit is permitted to count to a final value before the count register is reloaded.
wherein triggering of the watchdog timer circuit is avoided when the watchdog timer circuit is periodically reloaded, before a timeout period, by writing a magic value to a reload register, and wherein loading a value other than the magic value also causes the watchdog timer circuit to generate a triggered signal.

17. (Canceled)

18. (Original) The programmable logic integrated circuit of claim 17 wherein the timeout period is a time it takes for the watchdog timer circuit to count from an initial value to the final value.

19. (Original) The programmable logic integrated circuit of claim 16 wherein the plurality of logic array blocks are configured by programming SRAM memory cells.

20. (Original) The programmable logic integrated circuit of claim 16 wherein the plurality of logic array blocks are configured by programming volatile memory cells.

21. (Original) The programmable logic integrated circuit of claim 16 wherein the watchdog timer circuit comprises a reload register and a control register.

22. (Original) The programmable logic integrated circuit of claim 16 wherein each logic array block comprises a look-up table circuit.

23. (Currently Amended) ~~The programmable logic integrated circuit of claim 16~~ A programmable logic integrated circuit comprising:
a programmable logic portion of the integrated circuit comprising a plurality of logic array blocks, configurable to perform user logic, wherein the logic array blocks are arranged in rows and columns; and
an embedded processor portion of the integrated circuit, coupled to the programmable logic portion, comprising a watchdog timer circuit which is triggered if a count register of the watchdog timer circuit is permitted to count to a final value before the count register is reloaded.

wherein after the watchdog timer circuit is triggered, a reset circuit of the programmable logic integrated circuit effects loading of configuration data from an external source to reconfigure the programmable logic and embedded processor position of integrated circuit.

1 24. (Original) The programmable logic integrated circuit of claim 16 wherein
2 the embedded processor portion further comprises a central processing unit and an embedded
3 processor memory block, coupled together using a first bus.

1 25. (Original) The programmable logic integrated circuit of claim 24 wherein
2 the watchdog timer circuit is also coupled to the first bus.

1 26. (Original) The programmable logic integrated circuit of claim 24 wherein
2 the embedded processor further comprises a second bus, through which the memory block is
3 coupled to the programmable logic portion of the integrated circuit.

1 27. (Original) The programmable logic integrated circuit of claim 24 wherein
2 the external source is a Flash memory, EPROM memory, nonvolatile memory, or serial memory.

1 28. (Original) The programmable logic integrated circuit of claim 23 wherein
2 the configuration data is transferred to the programmable logic integrated circuit by using a serial
3 stream of bits.